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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/742,204	12/20/2000	Glen Fox	FUJ 00-01013RAM	7135

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,204	FOX ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12,14-17,19,20,22,24 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12,14-17,19,20,22,24 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *020204* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-10, 12, 14-17, 19-20, 22, 24 and 27 have been considered but are moot in view of the new ground(s) of rejection.

New Grounds of Rejection

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al. (U.S. Patent 6,682,772) in view of Mochizuki et al. (U.S. Patent No. 6,190,957).

In re claim 1, **Fox** discloses a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising: deposition of an electrically conductive bottom electrode layer **(FIG. 1: 20)** (col. 2, lines 42-47); deposition of a layer of ferroelectric dielectric material **(FIG. 1: 14)** (col. 3, lines 3-4); annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal (col. 2, line 63 to col. 3, line 10) at a first temperature (500 to 650° C); deposition of an electrically conductive top electrode layer **(FIG. 1: 12)** (col. 3, lines 14-21); annealing the layer of ferroelectric dielectric material with a second anneal (col. 3, line 10-21) at a second

temperature (700-750° C) higher than the first temperature, the second anneal changing the layer of ferroelectric material into grains having a columnar structure.

In re claims 1 and 8, **Fox** does not explicitly disclose wherein annealing the layer of ferroelectric dielectric material is being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer.

Mochizuki discloses a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of: deposition of an electrically conductive bottom electrode layer **(FIG. 24: 17)**; deposition of a layer of ferroelectric dielectric material **(FIG. 24: 18)**; annealing the layer of ferroelectric dielectric material (col. 34, lines 35-39); deposition of an electrically conductive top electrode layer **(FIG. 24: 19)**; annealing the layer of ferroelectric dielectric material with a second anneal, wherein the annealing process is being performed by rapid thermal annealing (RTA) (col. 34, lines 35-51) and performed after the step of deposition of an electrically conductive top electrode layer (col. 34, lines 30-51). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Fox and Mochizuki to enable the annealing process of Fox to be performed and furthermore to prevent deterioration in the characteristics of a ferroelectric capacitor and enabling process integration when a ferroelectric memory cell is manufactured (col. 6, lines 14-21).

In re claims 2, 3, **Fox** discloses wherein the electrically conductive bottom electrode layer **(FIG. 1: 20)** is a noble metal comprises platinum (col. 2, lines 42-62).

In re claim 4, **Fox** discloses wherein the ferroelectric dielectric layer **(FIG. 1: 14)** comprises PZT (col. 3, lines 2-13).

In re claims 5 and 6, **Fox** discloses wherein the electrically conductive top electrode layer **(FIG. 1: 12)** is a noble metal oxide comprises Iridium Oxide (IrO_x) (col. 3, lines 14-21).

In re claim 7, **Fox** discloses wherein the first anneal comprises a rapid thermal anneal at a temperature between 500 to 650 degrees Celsius (col. 3, lines 3-10).

In re claims 9 and 10, **Fox** discloses wherein the second anneal is performed at a temperature of between 700 to 750 degrees Celsius (col. 3, lines 10-21). There is no evidence indicating the annealing time duration is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

2. Claims 12, 14-16, 17, 19, 20, 22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al. (U.S. Patent 6,682,772) in view of Mochizuki et al. (U.S. Patent No. 6,190,957).

In re claim 12, **Fox** discloses a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising: deposition of an electrically conductive

bottom electrode layer **(FIG. 1: 20)** comprising a noble metal (col. 2, lines 42-47); deposition of a layer of ferroelectric dielectric material **(FIG. 1: 14)** (col. 3, lines 3-4); annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal (col. 2, line 63 to col. 3, line 10) in an environment comprising oxygen at a first partial pressure (col. 2, lines 42-62); deposition of an electrically conductive top electrode layer **(FIG. 1: 12)** comprising a noble metal oxide (col. 3, lines 14-21); annealing the layer of ferroelectric dielectric material with a second anneal (col. 3, line 10-21), the second anneal changing the layer of ferroelectric material into grains having a columnar structure, being performed in an environment comprising the oxygen having a second partial pressure less than the first partial pressure .

In re claims 12, 14, and 16, **Fox** does not explicitly disclose wherein annealing the layer of ferroelectric dielectric material is being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer.

Mochizuki discloses a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of: deposition of an electrically conductive bottom electrode layer **(FIG. 24: 17)**; deposition of a layer of ferroelectric dielectric material **(FIG. 24: 18)**; annealing the layer of ferroelectric dielectric material (col. 34, lines 35-39); deposition of an electrically conductive top electrode layer **(FIG. 24: 19)**; annealing the layer of ferroelectric dielectric material with a second anneal, wherein the annealing process is being performed by rapid thermal annealing (RTA) (col. 34, lines 35-51) and performed after the step of deposition of an electrically conductive top

electrode layer (col. 34, lines 30-51). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Fox and Mochizuki to enable the annealing process of Fox to be performed and furthermore to prevent deterioration in the characteristics of a ferroelectric capacitor and enabling process integration when a ferroelectric memory cell is manufactured (col. 6, lines 14-21).

In re claim 15, **Fox** discloses wherein the first partial pressure is less than ten percent of one atmosphere (col. 2, lines 42-62).

In re claims 17 and 20, **Fox** discloses wherein the first and second anneal is performed in an environment comprising a mixture of oxygen and inert gas (col. 2, lines 42-62).

In re claim 19, **Fox** discloses wherein the second partial pressure is less than five percent of one atmosphere (col. 2, lines 42-62).

In re claim 22, **Fox** discloses wherein the second anneal is performed at a temperature of between 700 to 750 degrees Celsius (col. 3, lines 10-21). There is no evidence indicating the annealing time duration is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05.

In re claim 24, **Fox** discloses wherein the step of depositing the ferroelectric dielectric layer (FIG. 1: 14) is performed by sputtering (col. 2, line 63 to col. 3, line 13).

3. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fox et al. (U.S. Patent 6,682,772) in view of Mochizuki et al. (U.S. Patent No. 6,190,957).

In re claim 27, **Fox** discloses a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising: deposition of an electrically conductive bottom electrode layer **(FIG. 1: 20)** comprising a noble metal (col. 2, lines 42-47); deposition of a layer of ferroelectric dielectric material **(FIG. 1: 14)** by sputtering method (col. 2, line 63 to col. 3, line13); annealing the layer of ferroelectric dielectric material to form perovskite phases with a first anneal (col. 2, line 63 to col. 3, line 10) at a first temperature (500 to 650° C); deposition of an electrically conductive top electrode layer **(FIG. 1: 12)** comprising (col. 3, lines 14-21); annealing the layer of ferroelectric dielectric material with a second anneal (col. 3, line 10-21) at a second temperature (700-750° C) higher than the first temperature, the second anneal changing the layer of ferroelectric material into grains having a columnar structure.

In re claim 27, **Fox** does not explicitly disclose wherein annealing the layer of ferroelectric dielectric material is being performed by rapid thermal annealing after the step of deposition of an electrically conductive top electrode layer.

Mochizuki discloses a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of: deposition of an electrically conductive bottom electrode layer **(FIG. 24: 17)**; deposition of a layer of ferroelectric dielectric material **(FIG. 24: 18)**; annealing the layer of ferroelectric dielectric material (col. 34, lines 35-39); deposition of an electrically conductive top electrode layer **(FIG. 24: 19)**; annealing the layer of ferroelectric dielectric material with a second anneal, wherein the annealing process is being performed by rapid thermal annealing (RTA) (col. 34, lines 35-51) and performed after the step of deposition of an electrically conductive top

electrode layer (col. 34, lines 30-51). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to combine the teaching of Fox and Mochizuki to enable the annealing process of Fox to be performed and furthermore to prevent deterioration in the characteristics of a ferroelectric capacitor and enabling process integration when a ferroelectric memory cell is manufactured (col. 6, lines 14-21).

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-10, 12, 14-17, 19-20, 22, 24 and 27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
April 16, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER